IN THE CLAIMS

Please cancel claims 1-22 without prejudice.

Please add claims 23-45 as follows:

~~Patent Claims~~WHAT IS CLAIMED IS:

1-22 (canceled)

23. (new) A semiconductor power switch comprising:

a source contact;

a drain contact;

a semiconductor structure provided between the source contact and the drain contact;

a gate used to control a current flow through the semiconductor structure between the source contact and the drain contact; and

wherein the semiconductor structure has a plurality of nanowires which are connected in parallel and are arranged in such a manner that each nanowire forms an electrical connection between the source contact and the drain contact.

24. (new) The semiconductor power switch of claim 23, wherein the length of the nanowires is ((0.2 μm) * (maximum value of the voltage (in V) which is applied to the semiconductor power switch)).

25. (new) The semiconductor power switch of claim 23, wherein the gate is implemented in the form of a gate layer which is provided between the source contact and the drain contact and is permeated by the nanowires, the nanowires being electrically insulated from the gate layer.

26. (new) The semiconductor power switch of claim 23, wherein the gate is implemented in the form of a plurality of gate bands whose longitudinal orientation respectively runs substantially perpendicular to the orientation of the nanowires and whose transverse orientation corresponds to the orientation of the nanowires, the nanowires being electrically insulated from the gate.

27. (new). The semiconductor power switch of claim 26, wherein the nanowires run within trenches provided between the gate bands.

28. (new) The semiconductor power switch of claim 26, wherein the gate bands and/or trenches are at an equal distance from one another.

29. (new) The semiconductor power switch of claim 27 , wherein tubes are provided within the trenches, at least one nanowire respectively running within the tubes.

30. (new). The semiconductor power switch of claim 27 , wherein insulation layers are provided between the trenches and the gate bands.

31. (new) The semiconductor power switch of claim 23, wherein the nanowires are insulated from one another.

32. (new) The semiconductor power switch of claim 23, wherein the nanowires are at an equal distance from one another.

33. (new) The semiconductor power switch of claim 25 , wherein the gate layer/the gate bands has/have a layer thickness/band width which is approximately 1/3 of the distance between the source contact and the drain contact.

34. (new) The semiconductor power switch of claim 26 wherein each gate band is split into a plurality of gate subbands which are insulated from one another, the gate subbands being arranged above one another and each being designed such that it can be driven individually.

35. (new) The semiconductor power switch of claim 34, wherein the gate subbands of a gate band are at an equal distance from one another.

36. (new). The semiconductor power switch of claim 35,

wherein vertical positions of the gate subbands of a gate band are shifted with respect to vertical positions of the gate subbands of an adjacent gate band.

37. (new) The semiconductor power switch of claim 23, wherein the nanowires are semiconducting carbon nanotubes.

38. (new) The semiconductor power switch of claim 23, wherein the nanowires comprise at least one or more of the following materials:

silicon;

germanium;

at least one of the III-V semiconductors BN, BP, BAs, AlN, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb;

at least one of the II-VI semiconductors ZnO, ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, HgSe, HgTe, BeS, BeSe, BeTe, MgS, MgSe; or

at least one of the compounds GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe;

at least one of the compounds CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI.

39. (new) The semiconductor power switch of claim 38 , wherein the nanowires are p-doped or n-doped.

40. (new) The method for improving the blocking effect of a semiconductor power switch comprising: providing a semiconductor power switch according to claim 34; and wherein, in the blocked state, selecting the potentials of the gate subbands in such a manner that the band gap structures of the nanowires assume an undulating shape.

41. (new) A method for producing a semiconductor power switch, the method comprising:

forming a layer structure on a drain contact, the layer structure having a first insulation layer, a gate layer which is arranged above the latter and a second insulation layer which is arranged above the gate layer;

forming trenches in the layer structure, the trenches reaching as far as the drain contact;

forming nanowires within the trenches; and

forming a source contact on the top side of the layer structure.

42. (new) The method of claim 41, comprising:

forming first trenches in the layer structure;

filling the first trenches with gate oxide;

forming second trenches in the gate oxide, the second trenches reaching as far as the drain contact;

forming nanowires within the second trenches; and

forming a source contact on the top side of the layer structure.

43. (new) The method of claim 41 , wherein the drain contact is composed of molybdenum or tantalum or contains these materials.

44. (new) The method of claim 43, comprising depositing a catalyst on the molybdenum or tantalum before the layer structure is formed or before the nanowires are formed.

45. (new) A semiconductor power switch comprising:

a source contact;

a drain contact;

means for providing a semiconductor structure between the source contact and the drain contact;

a gate used to control a current flow through the semiconductor structure means between the source contact and the drain contact; and

wherein the semiconductor structure means has a plurality of nanowires which are connected in parallel and are arranged in such a manner that each nanowire forms an electrical connection between the source contact and the drain contact